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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/540,423

06/24/2005

Toshio Kameshima

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EXAMINER

ELEY, JESSICA L

ART UNIT

PAPER NUMBER

2884

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/540,423	Applicant(s) KAMESHIMA, TOSHIO	
	Examiner JESSICA L. ELEY	Art Unit 2884	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 17-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 17-31 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 June 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>11/08/2007, 10/31/2006, 06/24/2005</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed on 24 June 2005.

Response to Amendment

Examiner acknowledges applicant's preliminary amendment filed 1 October 2007 which canceled claims 1-16 and added claims 17-31.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: phosphor layer **213** is missing for FIG. 10 as described in the specification on page 3 line 22. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 17-19, and 29-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Tashiro et al. 20020190215 A1 (henceforth referred to as Tashiro).

Regarding claim 17, Tashiro teaches a photoelectric converting apparatus (¶0020), on an insulating supporting substrate **103/104**, comprising:

A pixel comprising a photoelectric converting element **PD** (FIG. 14),

A resetting transistor **M2** wherein one of a source and a drain is connected to said photoelectric converting element **PD**, and the other of the source and the drain is connected to a resetting power source **RES**,

A readout transistor **M4** wherein a gate is connected to said photoelectric converting element **PD** and wherein one of a source and a drain is connected to a readout power source, and a selecting transistor **M3** connected to the other of the source and the drain of said readout transistor **M4**;

A signal line **S** connected to said pixel; and

Constant current source (Load current source) connected to said signal line and,

Readout means **N** connected to said signal line, wherein said constant current source is provided at a position on said signal line spaced from said readout means.

Regarding claims 18 and 31, Tashiro teaches the apparatus of claim 17, wherein said readout means **M4** includes an amplifier ($\P0074$) connected to said signal line **SEL1** and an analog multiplexer connected to said amplifier in the form of horizontal and vertical shift registers.

Regarding claim 19, Tashiro teaches the apparatus of claim 18, wherein said analog multiplexer is formed by a thin film transistor constituted of amorphous silicon or polysilicon on the same insulating substrate as that for said readout transistor.

Regarding claim 29, Tashiro teaches a photoelectric converting apparatus ($\P0020$), on an insulating supporting substrate **103/104**, comprising:

A two-dimensional array of a plurality of pixels each of which includes (FIG. 11):

A photoelectric converting element **PD** (FIG. 14),

A resetting transistor **M2** wherein one of a source and a drain is connected to said photoelectric converting element **PD**, and the other of the source and the drain is connected to a resetting power source **RES**,

A readout transistor **M4** wherein a gate is connected to said photoelectric converting element **PD** and wherein one of a source and a drain is connected to a readout power source, and

A selecting transistor **M3** connected to the other of the source and the drain of said readout transistor **M4**;

A plurality of common signal line **S** connected to said plural pixels; and

A constant current source (Load current source) connected to said common signal lines,

Wherein readout means **N** further connected to said common signal lines is further provided, and said constant current source is provided at a position on said common signal line spaced from said readout means rather than said plurality of pixels (FIG. 14).

Regarding claim 30, Tashiro teaches an X-ray image pickup system (FIG. 24) comprising a photoelectric converting apparatus according to any one of claims 17 and 31, an X-ray generating apparatus **6050** and control means **6070**,

Wherein said control means controls functions of said X-ray generating apparatus and said photoelectric converting apparatus thereby reading an X-ray image transmitted through an object (FIG. 24).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 20, and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro et al. 20020190215 A1 (henceforth referred to as Tashiro) as applied to claim 17 above, and further in view of Sakuragi US 2001/0033337 A1.

Regarding claim 20, Tashiro teaches the apparatus of claims 17, 18, or 19 but does not define the components of the constant current source. Sakuragi teaches a constant current source including a transistor of which a gate is connected to a power supply for said constant current source (¶0062). It would be obvious to a person of ordinary skill in the art at the time the invention was made to use the current source taught by Sakuragi as the current source since Tashiro does not disclose the specific elements of the current source thus leading one of ordinary skill to look for teachings as to the specific construction of a current source such as the one taught by Sakuragi, thus leading one of ordinary skill in the art to construct the current source from a transistor of which a gate is connected to a power supply.

Regarding claim 22, Tashiro and Sakuragi teach the apparatus of claims 17, 18, or 19. As can be seen in the teachings of Sakuragi the constant current source includes a constant current source transistor in which a gate and a source are mutually connected.

Regarding claim 23, neither Tashiro nor Sakuragi expressly teach connecting the gate and the source of the transistor in the constant current source by a resistor. However it would be obvious to one of ordinary skill in the art at the time the invention was made to use a resistor in this instance in order to bias any offset voltage that may occur.

Regarding claim 24, Tashiro and Sakuragi teach the apparatus of claims 17, 18, or 19. The apparatus taught by Tashiro utilizes amorphous silicon (¶0005) thus the resetting transistor,

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readout transistor; selecting transistor and said constant current source are formed in amorphous silicon.

Regarding claim 25, Tashiro and Sakuragi teach the apparatus of claims 17, 18, or 19. Tashiro further teaches the photoelectric converting apparatus comprising a scintillator (aka phosphor (¶0004) layer which absorbs a radiation and emits a light of wavelength region detectable by said photoelectric converting element (¶0071).

Regarding claim 26, Tashiro and Sakuragi teach the apparatus of claims 17, 18, or 19. Tashiro further teaches the photoelectric converting apparatus wherein said photoelectric converting element is a photodiode. Tashiro specify one particular type of photodiode, therefore it would be obvious to one of ordinary skill in the art at the time the invention was made to try using a PIN photodiode or MIS sensor as a person with ordinary skill has good reason to pursue the known options within his or her technical grasp and there are limited number of photodiodes that may be realized in silicon.

Claims 21, and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro et al. 20020190215 A1 (henceforth referred to as Tashiro) and Sakuragi US 2001/0033337 A1 as applied to claim 20 above, and further in view of NPL ELE343 Lab, Transistor modeling <http://www.ele.uri.edu/Courses/e/e343/lan/lab0/index.html> (henceforth referred to as ELE343).

Regarding claim 21, the teachings of Sakuragi regarding the use of a transistor as part of a constant current do not specify the relationship between the voltage of the drain-source, gate-

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source, and threshold voltage. However, the standard teachings in the art imply that the relation would be $V_{ds} > V_{gs} - V_{th}$ in order to result in a device that provides a constant current source, see page 3 of ELE343. Thus it would be obvious to a person of ordinary skill in the art at the time the invention was made to use the relation $V_{ds} > V_{gs} - V_{th}$, in which V_{ds} is a drain-source voltage, V_{gs} is a gate-source voltage and V_{th} is a threshold voltage for the current source of Sakuragi as this is necessary for standard operation of a transistor.

Regarding claim 22, as can be seen in the teachings of Sakuragi the constant current source includes a constant current source transistor in which a gate and a source are mutually connected.

Regarding claim 24, the apparatus taught by Tashiro utilizes amorphous silicon (§0005) thus the resetting transistor, readout transistor, selecting transistor and said constant current source are formed in amorphous silicon.

Regarding claim 23, neither Tashiro not Sakuragi expressly teach connecting the gate and the source of the transistor in the constant current source by a resistor. However it would be obvious to one of ordinary skill in the art at the time the invention was made to use a resistor in this instance in order to bias any offset voltage that may occur.

Regarding claim 25, Tashiro further teaches the photoelectric converting apparatus comprising a scintillator (aka phosphor (§0004) layer which absorbs a radiation and emits a light of wavelength region detectable by said photoelectric converting element (§0071).

Regarding claim 26, Tashiro further teaches the photoelectric converting apparatus wherein said photoelectric converting element is a photodiode. Tashiro specify one particular type of photodiode, therefore it would be obvious to one of ordinary skill in the art at the time the

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invention was made to try using a PIN photodiode or MIS sensor as a person with ordinary skill has good reason to pursue the known options within his or her technical grasp and there are limited number of photodiodes that may be realized in silicon.

Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro et al. 20020190215 A1 (henceforth referred to as Tashiro), as applied to claims 17, 18, or 19, and Tashiro, Sakuragi US 2001/0033337 A1, and NPL ELE343 Lab, Transistor modeling <http://www.ele.uri.edu/Courses/e343/lan/lab0/index.html> (henceforth referred to as ELE343) as applied to claim 21, and in further view of Kameshima et al. US 20010033336 A1 (henceforth referred to as Kameshima).

Regarding claims 27 and 28, the detector taught by Tashiro and Sakuragi do not use direct conversion photoelectric converting elements. However, such elements are well known in the art. For example Kameshima teaches direct conversion when waves such as X-rays are being detected, using materials such as amorphous selenium, lead (II) iodide, and gallium arsenide (¶0026). It would be obvious to one of ordinary skill in the art at the time the invention was made to use the direct conversion element taught by Kameshima as the photoelectric converting element in Tashiro as this negate the need for an additional scintillation layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSICA L. ELEY whose telephone number is (571)272-9793. The examiner can normally be reached on Monday - Thursday 8:00-6:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. L. E./
Examiner, Art Unit 2884
/Christine Sung/
Primary Examiner, Art Unit 2884